CODE: 17CD04106

M. Tech I Year I Semester Supplementary Examinations, May 2018

LOW POWER VLSI DESIGN

(VLSISD)

Time : 3 hours Max Marks : 60

Answer all **five** units. (5 x 12 = 60 Marks)

UNIT-I

1. (a) Elaborate on dynamic and short circuit power dissipation.

(b) Write about transistor leakage mechanism.

OR

2. Explain the following

(a) Fowler- Nordheim tunneling

(b) Gate induced drain leakage

(c) Punch- through

UNIT-II

3. (a) Influence of voltage scaling on power delay.

(b) Explain about VT CMOS.

OR

4. Briefly explain about

(a) MT CMOS

(b) Parallel Processing

UNIT-III

5. (a) Design a CMOS full address circuit.

(b) Elaborate on CSA.

OR

6. Design and explain different XOR/XNOR structures.

UNIT-IV

7. (a) Explain shift/add multiplication algorithms.

(b) Elaborate on modified booth algorithm.

OR

8. Draw the basic building block of Wallace Tree Multiplier.

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UNIT-V

9. (a) Explain low power ROM technology.

(b) Give a note on future trend and development of DRAM.

OR

10. (a) With a neat sketch, explain the block diagram of Precharge and Equalization circuit.

(b) Discuss Self-Refresh circuit with neat diagram.

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