CODE: 17CD04104

M. Tech I Year I Semester Supplementary Examinations, May 2018

HARDWARE DESCRIPTION LANGUAGES
(VLSISD)

Time : 3 hours Max Marks : 60

Answer all **five** units. (5 x 12 = 60 Marks)

UNIT-I

1. (a) Illustrate with an example the syntax for
i. Module declaration
ii. Module instantiation
iii. Parameterized Modules

(b) With relevant examples explain Pin-to-Pin delay's

OR

2. (a) Explain the Verilog module for a structural description of a Half Adder

(b) Model the propagation delay of a NAND Gate

UNIT-II

3. (a) What are Blocking Assignments, With an example explain the syntax of Blocking Assignment

(b) Explain the use of the following with an example
i. begin……end
ii. for loop
iii. while loop

OR

4. (a) What are Conditional statements, explain the syntax of if statement and association of else in nested if statements

(b) With an example explain the syntax of
i delay_control
ii event_control

UNIT-III

5. (a) Implement the behavioral model of Mealy state machine to design a synchronous Finite State Machine

(b) Explain in brief the styles for synthesizable Combinational Logic

OR

6. (a) Design a 4-bit ripple counter

(b) Design a 3-bit UP/DOWN counter

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UNIT-IV

7. (a) Explain in detail the two MOS switches

(b) Draw the circuit diagram of switch level CMOS 2-input NOR gate and develop its source code using Verilog HDL

OR

8. (a) Explain the primitive gate output strength values relevant to strength modeling in Verilog HDL

(b) Draw the circuit diagram, the logic circuit of a 2- input CMOS NAND gate and write the Verilog HDL code

UNIT-V

9. (a) Explain with relevant diagrams the Top Down design approach in digital Systems

(b) Differentiate between VHDL and Verilog with suitable examples

OR

10. (a) Explain the top- level design of ALU using VHDL with its function table

(b) Explain the following design procedures in VHDL
i Design entity
ii Synthesis
iii Optimization

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