CODE: 17CD04106

M. Tech I Year I Semester Regular Examinations, February 2018

LOW POWER VLSI DESIGN

(VLSISD)

Time : 3 hours Max Marks : 60

Answer all **five** units. (5 x 12 = 60 Marks)

UNIT-I

1. (a) What are the sources of power dissipation in Digital CMOS circuits? With usual notation derive the equation for short circuit power dissipation in a CMOS inverter. Discuss the techniques to minimize the short circuit power dissipations.

(b) Illustrate the Leakage Power dissipation in CMOS inverter and the various leakage current components in MOSFET with relevant figure and equations for the same

OR

2. (a) Explain the causes and effects of punch through. Describe the methods to control punch through.

(b) Explain the need for low power VLSI design. Illustrate glitching power dissipation, its causes and how it can be reduced

UNIT-II

3. (a) Illustrate the features of variable-threshold CMOS (VTCMOS) inverter circuit with a neat figure

(b) Illustrate the Parallel processing approach in designing the low power CMOS logic design with relevant figure and equations

OR

4. (a) Explain the different techniques used for the reduction of switched capacitance.

(b) Examine the effects of reducing the power supply voltage V_{DD} upon switching power consumption and dynamic performance of the gate.

UNIT-III

5. (a) Interpret the role of full adders in VLSI design applications? Draw the logic circuit of conventional CMOS full adder along with its truth table and logic functions for sum and carry. Also explain the need, working and logic structure of a fast full adder

(b) Explain the features of Condition Sum Adders (COS) with a neat figure of the schematic diagram if 4-bit COS

OR

6. (a) Explain the basic theory, working and operation of Carry Save Adders (CSA) with a neat figure of 4-operand CSA

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(b) Discuss the low-voltage low-power design techniques with respect to following
   i. Trends of technology and power supply voltage

Low voltage low power logic styles

UNIT-IV

7. (a) Illustrate the features, architecture, performance and speed considerations of Braun multiplier

(b) Explain the features of n x n-bit modified Booth multiplier with a neat figure of its block diagram. Also explain the working, structure of Booth encoder with a neat figure

OR

8. (a) Illustrate the multiplication of unsigned numbers using mathematical equations and explain the different categories of multiplier architecture classification

(b) Explain the role and working of 4:2 compressors with a neat figure of its schematic diagram and equivalent circuit. Also explain the Wallace tree construction

UNIT-V

9. (a) Sketch a neat figure of the basic ROM architecture and explain its working. Explain the low power techniques for ROM at the architecture level

(b) Compare and comment on the race between 6T and 4T memory cells with a neat figure of static 4T memory cells with different loads.

OR

10. (a) Illustrate the SRAM architecture with a neat figure of its block diagram and explain its read and write operation

(b) Sketch a neat figure of the block diagram of the refresh trigger signal generator for the self-refresh circuit in DRAM and explain its various blocks

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